CLAIMS

What we claim is:

1. An emulated EEPROM memory device, comprising a memory macrocell which is embedded into an integrated circuit having a microcontroller, the memory macrocell including a Flash memory structure formed by a predetermined number of sectors, wherein at least two sectors of the Flash memory structure are structured to emulate EEPROM byte alterability.

2. The emulated EEPROM memory device according to claim 1, wherein said EEPROM byte alterability is emulated by hardware means.

3. The emulated EEPROM memory device according to claim 1, wherein 8 Kbyte of the Flash memory structure are used to emulate 1 Kbyte of an EEPROM memory portion.

4. The emulated EEPROM memory device according to claim 1, wherein first and second EEPROM emulated sectors are each divided in a predetermined number of blocks of the same size and each block is divided in pages.

5. The emulated EEPROM memory device according to claim 1, wherein a state machine is provided for controlling an address counter which is output connected to an internal address bus running inside the memory macrocell, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update.

6. The emulated EEPROM memory device according to claim 5, wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase.

7. The emulated EEPROM memory device according to claim 1, wherein Flash and EEPROM memories operations are controlled through a register interface mapped into the memory.

8. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode.

9. The method according to claim 8, wherein at a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to the another EEPROM sector.

10. A Flash memory device for emulating an EEPROM, comprising:

first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second

Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and

a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and

a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.

11. The Flash memory device of claim 10 wherein the first and second Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second Flash memory portion.

12. The Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.

13. The Flash memory device of claim 12 wherein the plurality of Flash memory portions include two Flash memory portions, each with four memory blocks, each memory block including 64 memory pages each with 16 memory locations that are able to store a data byte.

14. The Flash memory device of claim 10, further including a third Flash memory portion not organized to emulate the EEPROM.

15. The Flash memory device of claim 14, further including first and second sense amplifiers, the first sense amplifier being coupled to, and structured to read, the first and second Flash memory portions and the second sense amplifier being coupled to, and structured to read, the third Flash memory portion.

16. A method of emulating an EEPROM using Flash memory, the method comprising:

dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;

assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors;

in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and

in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.

17. The method of claim 16, further comprising, in response to a third write instruction to write to the selected page address when a most recent write instruction to write to the selected page address was executed by writing to a last memory block of the first memory sector, executing the third write instruction by writing to a first memory block of the second memory sector.

18. The method of claim 16 wherein all memory pages sharing a same page address constitute a set of memory pages, the number of sets of memory pages equaling how many memory pages are in each memory block, the method further comprising:

assigning to each set of memory pages of the first and second memory sectors a page pointer that reflects which memory page in the set has been most recently updated; and

in response to each write instruction requesting to write data to the selected page address, determining which page pointer is associated with the selected page address, determining from the page pointer associated with the selected page address which memory page of the set of memory pages assigned the selected page address is next to be updated, and writing the data in the memory page that is determined to be the next memory page to be updated.

19. The method of claim 16, further comprising erasing the second memory sector while updating memory pages of the first memory sector.

20. The method of claim 19 wherein the erasing act is performed in plural erase phases, with each of the erase phases being triggered by writing data in the first memory sector.